REMARKS

When the Examiner begins reviewing this amendment, she is respectfully requested to contact the undersigned at the number set forth below to arrange an interview for this case.

Claims 11 and 12 were rejected under 35 U.S.C. § 103 (a) as being unpatentable over Applicant's prior art figures 1a- 1d. From the Examiner's remarks it appears that it is actually Figs. 1a, 1b and 1c that are being asserted as constituting prior art.

It is noted that the application discusses the panel of Figs 1a, 1b as well as the device of Fig. 1c in the background section. However, the undersigned has confirmed with the inventors that to the best of their knowledge, the illustrated panel structure of Figs. 1a, 1b as well as the devices of Fig. 1c are NOT prior art. This has necessitated the amendments to the specification, which are included herewith. It is respectfully submitted that the amendments to the specification do not present any new matter.

As Figs 1a, 1b and 1c are not prior art, but rather an embodiment of applicants' invention, the rejection under 35 U.S.C. § 103 (a) should be withdrawn.

Claim 16 was objected to as being dependent upon a rejected base claim, but was believed to be allowable if rewritten in proper independent form. Applicants believe they have amended claim 16 into proper independent form and that claim 16 as amended should be allowed.

The Examiner has rejected claims 13 through 15 and 18 through 44 under 35 U.S.C. §102(b) as anticipated by Lin et al., U.S. Patent No. 5,273,938 (Lin).

The present application describes a novel method of packaging integrated circuits. As described therein, a lead frame is provided which has a two dimensional array of device areas. In the packaging process, integrated circuit dice are positioned in the device areas and electrically coupled to their associated contacts. A plastic cap is then formed over the array so the cap covers a two dimensional array of device areas while leaving bottom surfaces of the contacts exposed. Thus, an array of devices are encapsulated under a single cap prior to

singulation. The devices may then be singulated (typically by sawing) thereby providing a very cost effective arrangement for packaging integrated circuits.

The various claims are directed at novel structures that are particularly well suited for use in the described packaging approach, or are intermediate or final components in the described packaging approach.

The Lin reference only describes the fabrication of a single IC module at a given time. Lin does describe placing more than one IC die on a conductive trace formed on a transfer material, but these several IC dies all form together a single semiconductor device. It is accurate to state that the devices fabricated using the teachings of Lin are all relatively expensive, as each finished device is described as having several IC dies within it. Indeed, Lin mentions that each finished semiconductor device requires several encapsulation steps: a first encapsulation step to package the dice mounted on a first top surface of the conductive traces and at least a second encapsulation step to package the dice mounted on the other side of the conductive traces. At a minimum, the method taught in Lin requires at least two encapsulation steps to complete a single semiconductor device. This is in sharp contrast to the present inventions. Therefore, it is not surprising that the structures disclosed by Lin are somewhat different that the structures described in the present application and as set forth in the currently pending claims.

For example, claim 13 has been amended to make it clear that the integrated circuit package is one of a plurality of integrated circuit packages fabricated simultaneously on a lead frame having a two dimensional array of die attach pads and conductive leads formed thereon that are positioned under the plastic encapsulation. It is respectfully submitted that this structure is not disclosed or reasonably suggested by Lin.

Claim 18 is directed at a lead frame suitable for use in semiconductor packaging and requires a matrix of tie bars that extend in substantially perpendicular rows and columns to define a two dimensional array of immediately adjacent device areas separated only by the tie bars, each device area being suitable for use in an independent integrated circuit package. Again, it is respectfully submitted that this structure is not disclosed or reasonably suggested by Lin.

Claim 26 is directed at a panel assembly suitable for use in packaging an array of integrated circuits simultaneously. The panel assembly includes a lead frame panel patterned to

define at least one two dimensional array of adjacent device areas that are each suitable for use as part of an independent integrated circuit package. Claim 26 also requires a molded cap that substantially uniformly covers the array of device areas while leaving bottom surfaces of the conductive contacts exposed to facilitate electrical connection to external components, wherein encapsulation material that forms the molded cap is exposed at a bottom surface of the panel of integrated circuits to physically isolate the contacts. Again, it is respectfully submitted that this structure is not disclosed or reasonably suggested by Lin.

Claims 34 and 36 are directed at the finished products. These claims specifically require that the plastic encapsulation has a rectangular footprint with side walls that are substantially perpendicular to a bottom surface of the integrated circuit package. They also require that the side walls of the plastic encapsulation form sharp corners where they meet. It is acknowledged that these claims recite a structure that at first glance appears to read very closely on the structure illustrated in Fig. 1 of Lin. However, it is respectfully submitted that Figure 1 is a diagrammatic illustration of the structure rather than the actual geometry of the structure. Specifically, at col. 3, line 57 – col. 4, line 8, Lin describes that the package body 20 is formed by injection molding, transfer molding or glob topping processes. It is respectfully submitted that in order to accomplish injection or transfer molding, the edges of the molds must be tapered somewhat and the corners of the mold must be slightly rounded (as opposed to sharp). Otherwise, it is not practical to withdraw the molded components from the mold. This feature of molding is well know in the industry and it is common to diagrammatically represent devices as rectangular structures when in fact they do not have truly perpendicular side walls. It is also common to diagrammatically represent devices as having sharp corners, when they do not. In contrast, the claimed devices, which were formed by sawing, do truly have substantially perpendicular side walls and do truly have very sharp corners. In view of the foregoing, it is respectfully submitted that claims 34 and 36, as presently presented are patentable over the Lin reference.

Claim 38 is directed at a panel assembly suitable for use in packaging an array of integrated circuits. The panel assembly has a lead frame panel patterned to define at least one two dimensional array of adjacent device areas that are each suitable for use as part of an independent integrated circuit package. A molded cap is provided that covers the array of device areas while leaving bottom surfaces of the contacts exposed to facilitate electrical connection to external components. Again, it is respectfully submitted that such an arrangement is not disclosed or reasonably suggested by Lin.

In view of the foregoing, it is respectfully submitted that all pending claims are allowable and the Applicant respectfully requests a Notice of Allowance for this application from the Examiner. As pointed out above, the Examiner is respectfully requested to contact the undersigned to arrange an interview when this case is picked up for examination. If any fees are due in connection with the filing of this amendment, such fees may be charged to our deposit account.

Respectfully submitted,
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MARKED UP VERSION OF THE AMENDED SPECIFICATION

Please **replace** the first paragraph of the Detailed Description section of the application, beginning on page 4, line 13 and continuing to page 5, line 7 of the specification with the following three **amended** paragraphs. It is noted that the first paragraph being inserted is taken primarily from the former first paragraph of the "Related Art" that was deleted, the second paragraph is new, and the third paragraph makes minor changes in the former first paragraph of the Detailed Description.

[The present invention employs a rigid support fixture during the manufacturing process to enable the use of lead frames in the chip scale IC packages. An embodiment of a support fixture 200 includes a rigid frame 210 and an adhesive pad 220, as shown in the exploded isometric diagram of Fig. 2a. Because the pad 220 is affixed along the border t frame 210, it maintains sufficient tension to provide a stable supporting surface for a lead frame panel 110. By making pad 220 out of a thin, flexible, and electrically non-conductive material, it provides a support structure that will not interfere with the conventional manufacturing processes used in IC package assembly. The size of the interior opening of the frame 210 is large enough to allow lead frame panel 110 to be supported by pad 220. Multiple IC chips 130 are then installed and wire bonded on lead frame panel 110, as shown in Fig. 2b. Subsequent encapsulation of IC chips 130 in protective casings proceeds as in conventional lead frame processing. If a molded protective casing is to be applied, and encapsulant dam 240 can be constructed around the perimeter of lead frame panel 110. Dam 240 can be made of any substantially rigid substance, including premolded plastic, epoxy, or tape, and serves to prevent flow of encapsulant material beyond the boundaries of lead frame panel 110. Alternatively, containing measures for encapsulant material could be incorporated into the dispensing mechanism. Once encapsulation is complete, support fixture 200 can be removed, either before of after singulation.]

Generally, an integrated circuit (IC) package encapsulates an IC chip, or die, in a protective casing and also provides power and signal distribution between the IC chip and an external printed circuit board (PCB). A metal lead frame can be used to provide the electrical paths for that distribution. A lead frame panel suitable for use in accordance with the present invention is illustrated in Fig. 1a. For production purposes, a lead frame panel 110 made up of multiple lead frames 120 is etched or stamped from a thin sheet of metal, as shown in Fig. 1a. An IC chip 130 is then mounted and wire bonded to each lead frame 120, as shown in Fig. 1b. Wire bonding is typically performed using fine gold wires

140. As illustrated in Fig. 1c, each IC chip 130 is then encapsulated in a protective casing 160 which may be formed by dispensing and molding a layer of encapsulant material over all IC chips 130. Next lead frames 120 are cut apart, or singulated to produce individual IC packages 190.

Referring again to Fig. 1a, panel 110 includes a two dimensional array of device areas. Each device area has a plurality of contacts 112 and a die attach pad 114. The panel has a grid of tie bars 115 that extend in perpendicular rows and columns to define the device area. The tie bars 115 carry the contacts 112 and die attach pads 114.

The embodiment shown in Fig. 2a employs a rigid supporting fixture during the manufacturing process to enable the use of lead frames in chip scale IC packages. An embodiment of a support fixture 200 includes a rigid frame 210 and an adhesive pad 220, as shown in the exploded isometric diagram of Fig. 2a. Because pad 220 is affixed along its border to frame 210, it maintains sufficient tension to provide a stable supporting surface for a lead frame panel 110. By making pad 220 out of a thin, flexible, and electrically non-conductive material, it provides a support structure that will not interfere with the conventional manufacturing processes used in IC package assembly. The size of the interior opening of frame 210 is large enough to allow lead frame panel 110 to be fully supported by pad 220. Multiple IC chips 130 are then installed and wire bonded on lead frame panel 110, as shown in Fig. 2b. Subsequent encapsulation of IC chips 130 in protective casings proceeds as in conventional lead frame processing. If a molded protective casing is to be applied, an encapsulant dam 240 can be constructed around the perimeter of lead frame panel 110. Dam 240 can be made of any substantially rigid substance, including premolded plastic, epoxy, or tape, and serves to prevent flow of encapsulant material beyond the boundaries of lead frame panel 110. Alternatively, containing measures for encapsulant material could be incorporated into the dispensing mechanism. Once encapsulation is complete, support fixture 200 can be removed, either before or after singulation.

MARKED UP VERSION OF THE AMENDED CLAIMS

13. (Once Amended) An integrated circuit package for accommodating a semiconductor die, comprising:

a planar lead frame comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads; and

an adhesive pad removably attached to said integrated circuit package, covering said lower surface of said die attach pad and said lower surfaces of said conductive leads, and

wherein said integrated circuit package is one of a plurality of integrated circuit packages fabricated simultaneously on said lead frame, said lead frame comprising a two dimensional array of die attach pads and conductive leads that are positioned under the plastic encapsulation, and wherein said adhesive pad supports the array of die attach pads and conductive leads prior to singulation of the plurality of integrated circuit packages.

15.(Once Amended) An integrated circuit package as in Claim [14] 13, wherein said lead frame is fabricated on a metal panel.

16.(Once Amended) An integrated circuit package [as in Claim 15,] for accommodating a semiconductor die, comprising:

a planar lead frame fabricated on a metal panel comprising (a) a die attach pad supporting said semiconductor die on an upper surface of said die attach pad, and (b) substantially planar conductive leads positioned around an outer periphery of said die attach pad, wherein each of said conductive leads has a lower surface that is substantially coplanar with said lower surface of said die attach pad, said upper and lower surfaces of said die attach pad being located on opposite sides of said die attach pad;

a plurality of bond wires each coupling one of said conductive leads to a corresponding bonding pad on said semiconductor die; and

a plastic encapsulation enclosing said semiconductor die, said bond wires and said lead frame, exposing at a lower surface of said plastic encapsulation said lower surface of said die attach pad and said lower surfaces of said conductive leads; and

an adhesive pad removably attached to said integrated circuit package, covering said lower surface of said die attach pad and said lower surfaces of said conductive leads,

wherein said integrated circuit package is one of a plurality of integrated circuit packages fabricated simultaneously from said lead frame, said lead frame comprising an array of die attach pads and conductive leads, and said adhesive pad supports said die attach pads and said conductive leads prior to singulation of said plurality of integrated circuit packages and further comprising an encapsulant dam provided to enclose said array of die attach pads and conductive leads.

17. (Once Amended) An integrated circuit package as in Claim [14] 13, wherein said array of die attach pads and conductive dies is being arranged in a regular pattern so as to allow singulation of said integrated circuit packages by sawing through said plastic encapsulation and said conductive leads at predetermined positions.

26. (Once Amended) A panel assembly suitable for use in packaging an array of integrated circuits simultaneously, the panel assembly having top and bottom surfaces and comprising:

a lead frame panel formed from a conductive sheet, the lead frame panel being patterned to define at least one two dimensional array of adjacent device areas, each device area being

suitable for use as part of an independent integrated circuit package and including a die and a plurality of contacts positioned around and electrically connected to the die; and

a molded cap that substantially uniformly covers the array of device areas while leaving bottom surfaces of the conductive contacts exposed to facilitate electrical connection to external components, wherein encapsulation material that forms the molded cap is exposed at a bottom surface of the panel of integrated circuits to physically isolate the contacts.

34. (Once Amended) An integrated circuit package comprising:

a planar lead frame including a die attach pad and a plurality substantially planar conductive contacts positioned around an outer periphery of the die attach pad, wherein the die attach pad and the conductive contacts are substantially co-planar;

a die mounted on the die attach pad;

a plurality of bond wires, each bond wire coupling one of the conductive contacts to a corresponding bonding pad on the die; and

a plastic encapsulation covering the die, the bond wires and the lead frame while leaving bottom surfaces of the die attach pad and the conductive contacts exposed, wherein encapsulation material that forms the plastic encapsulation mechanically supports the conductive contacts and is exposed at a bottom surface of the lead frame to physically isolate the conductive contacts, wherein the plastic encapsulation has a rectangular footprint with side walls that are [substantially] perpendicular to a bottom surface of the integrated circuit package and wherein the side walls of the plastic encapsulation form sharp corners where they meet.

36. (Once Amended) An integrated circuit package comprising:

a planar lead frame including a die attach pad and a plurality substantially planar conductive contacts positioned around an outer periphery of the die attach pad, wherein the die attach pad and the conductive contacts are substantially co-planar;

a die mounted on the die attach pad;

a plurality of bond wires, each bond wire coupling one of the conductive contacts to a corresponding bonding pad on the die;

a plastic encapsulation covering the die, the bond wires and the lead frame while leaving bottom surfaces of the die attach pad and the conductive contacts exposed, wherein encapsulation material that forms the plastic encapsulation is exposed at a bottom surface of the lead frame to physically isolate the conductive contacts; and

an adhesive pad removably attached to the a bottom surface of the lead frame, thereby covering the exposed bottom surfaces of the die attach pad, the conductive contacts and the plastic encapsulation; and

wherein the plastic encapsulation has a rectangular footprint with side walls that are substantially perpendicular to a bottom surface of the integrated circuit package, and the side walls of the plastic encapsulation form sharp corners where they meet.